Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): An arithmetic unit comprising:

a memory for storing data;

an arithmetic logic unit for executing a predetermined arithmetic operation with respect to a [[the]] data [[read]] from memory, the data being grouped into one of several patterns;

a register for temporarily storing the data read from the memory; and

a combining circuit for receiving [[an]] a first output data from the arithmetic logic unit and a second output data from the register, and outputting data which is provided by replacing a part of the first output data ~~read from the memory with said received~~ and a part of the second output data based on the pattern of the data.

Claim 2 (Currently Amended): An arithmetic unit according to claim 1, wherein, when the parts [[part]] of the first and second output data ~~read from the memory is~~ are replaced with an arithmetic result derived by the arithmetic logic unit, the combining circuit shifts a position of data to be replaced by a predetermined number of bits every time an operation process is executed.

Claim 3 (Original): An arithmetic unit according to claim 1, wherein the memory includes a plurality of memory blocks.

Claim 4 (Previously Presented): An arithmetic unit according to claim 1, wherein the arithmetic logic unit divides a carry signal in response to a division signal received thereto.

Claim 5 (Original): An arithmetic unit according to claim 1, further comprising a shifter for shifting data received from the memory and outputting the shifted data to the arithmetic logic unit.

Claim 6 (Original): An arithmetic unit according to claim 1, further comprising an accumulator for temporary storing data output from the arithmetic logic unit.

Claim 7 (Currently Amended): An arithmetic unit comprising:

a memory for storing data;

an arithmetic logic unit capable of prohibiting ripple carry to an upper digit when a carry signal instructs a carry at an arbitrary bit position;

a register capable of storing data to be used in the arithmetic logic unit before an arithmetic operation is executed in the arithmetic logic unit; and

a combining circuit for receiving [[an]] a first output data from the arithmetic logic

unit and a second output data from the register, and outputting data which is provided by replacing a part of the data read from memory with ~~said received~~ the first output data.

Claim 8 (Previously Presented): An arithmetic unit according to claim 7, wherein, when the part of the data read from the memory is replaced with an arithmetic result derived by the arithmetic logic unit, the combining circuit shifts a position of data to be replaced by a predetermined number of bits every time an operation process is executed.

Claim 9 (Original): An arithmetic unit according to claim 7, wherein the memory includes a plurality of memory blocks.

Claim 10 (Previously Presented): An arithmetic unit according to claim 7, wherein the arithmetic logic unit divides a carry signal in response to a division signal received thereto.

Claim 11 (Original): An arithmetic unit according to claim 7, further comprising a shifter for shifting data received from the memory and outputting the shifted data to the arithmetic logic unit.

Claim 12 (Original): An arithmetic unit according to claim 7, further comprising an accumulator for temporary storing data output from the arithmetic logic unit.

Claims 13-20 (Canceled)